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RF-3581-82

M. Sc. (Part - II) Examination

April / May – 2010

Physics : Paper - III

(Spl. Electronics - II)

(Micro Electronics & Computers & Microprocessor)

Time : **3** Hours] [Total Marks : **70**

RF-3581

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ M. Sc. - 2

Name of the Subject :

☛ PHYSICS - 3

☛ Subject Code No. : 3 5 8 1 ☛ Section No. (1, 2,.....) : 1

Seat No. :

Student's Signature

(2) Figures to the right indicate full marks of the question.

(3) Symbols have their usual meaning.

(4) Answers to the two sections must be written in separate answer books.

1 (a) How an NMOS can use as an Analog switch? Give such circuit and explain its operation. **4**

(b) Explain the following terms: **3**

(i) Depleation load inverter

(ii) Current Source

(iii) Signal flow graph

(c) Construct three input NAND gate using NMOs transistor. Give their switch analogy and obtain Truth Table. 4

2 (a) Explain Emitter Coupled Logic Circuit in detail. List their limitations. 4

(b) What is FAMOS? List the applications of FAMOS. Explain such application in detail. **3**

(c) Two 16 Kb (2048x8) ROMs are available. Show how to connnect these so as to obtain **5**
(a) a 32 kb (2048 × 16) ROM and
(b) a 32 kb (4096 × 8) ROM

OR

2 (a) Why three stage architecture is required for BIFET BIMOS op-Amp? Explain such architecture in detail. **4**

(b) What is stability? Explain Nyquist's Criterion for stability test. **3**

(c) Give the architecture for CMOS transmission gate. Explain its operation using clock pluses. **5**

3 (a) Give the Schematic diagram of a Regulated Power supply. List the limitations of Pass regulator. **4**

(b) Sketch the topology for a generalized resonant circuit oscillator, using impedances Z_1, Z_2 and Z_3. At what frequency will the circuit oscillate?

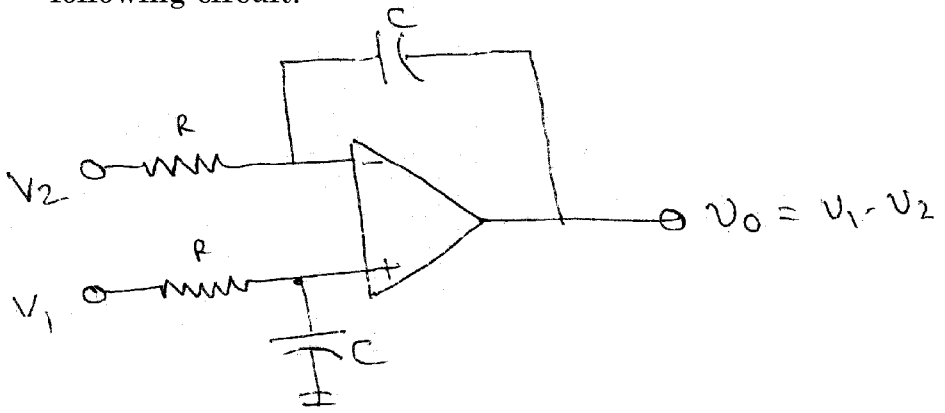
(c) A two pole feedback amplifier is to be designed with $T_0 = 90$ and $W_H = 10^7$ rad/s. Determine W_1, W_2 and ϕ_m for the value of Q is 0.500. **5**

OR

3 (a) Define Electron per Bit of a CCD. Explain charge transfer in 3 phase CCD using suitable example **4**

(b) Explain the high frequency response of an Common Emitter Amplifier Stage. **3**

(c) Show a switched Capacitor equivalent of the following circuit. **5**



RF-3582

Instructions :

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Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ M. Sc. - 2

Name of the Subject :

☛ PHYSICS - 3

☛ Subject Code No. : 3 5 8 2 ☛ Section No. (1, 2,.....) : 2

Seat No. :

Student's Signature

(2) Figures to the right indicate full marks of the question.
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(4) Answers to the two sections must be written in separate answer books.

4 (a) Briefly explain the importance of `NOP' instruction of 8085 microprocessor. **2**

(b) Convert following numbers into Decimal and BCD. **2**
(i) 1010_2
(ii) 0011_2

(c) What do you understand by the term "interrupt Priority"? **2**

(d) What is the function of SOD pin of 8085 microprocessor? **2**

(e) Using only NOR gates, design a 3-line to 8-line decoder. **3**

5 (a) Explain with example 1s and 2s complement method to represent negative numbers in digital computers. **6**

(b) What is the difference between a binary adder and BCD adder? Design a 4-bit BCD adder and with example explain its operation. **6**

OR

5 (a) In context to memory, explain the term 'dimension'. Using two dimensional basic memory cells, design a 4×3 memory block and explain its operation. **6**

(b) With logic `1' as starting condition, draw the waveform of the digital pattern 0101001_2 in following recording schemes : **6**

(i) NRZ

(ii) NAZ Mark and

(iii) NRZ B_1 phase mark.

6 (a) Draw the block diagram of 8085 microprocessor and with suitable example the role of program counter register (PC) and flag register. **6**

(b) What does the following instruction of 8085 microprocessor do? **6**

(i) RET

(ii) JNC

(iii) DCX B

(iv) RRC

(v) LXI H

(vi) POP PSW

OR

6 (a) What is post? Draw the block diagram of 8255 PPI. Giving control word format of 8255 PPI, explain its different modes of operation. **6**

(b) Write an assembly language program to generate square wave on PC_4 and PC_7 using BSR mode of 8255 PPI. **6**
(Assume 1FH as control register address and delay subroutine is available at 2080H).